TS256MLK64V1U

240PIN DDR3 1066 Unbuffered DIMM
2GB With 128Mx8 CL7

Description

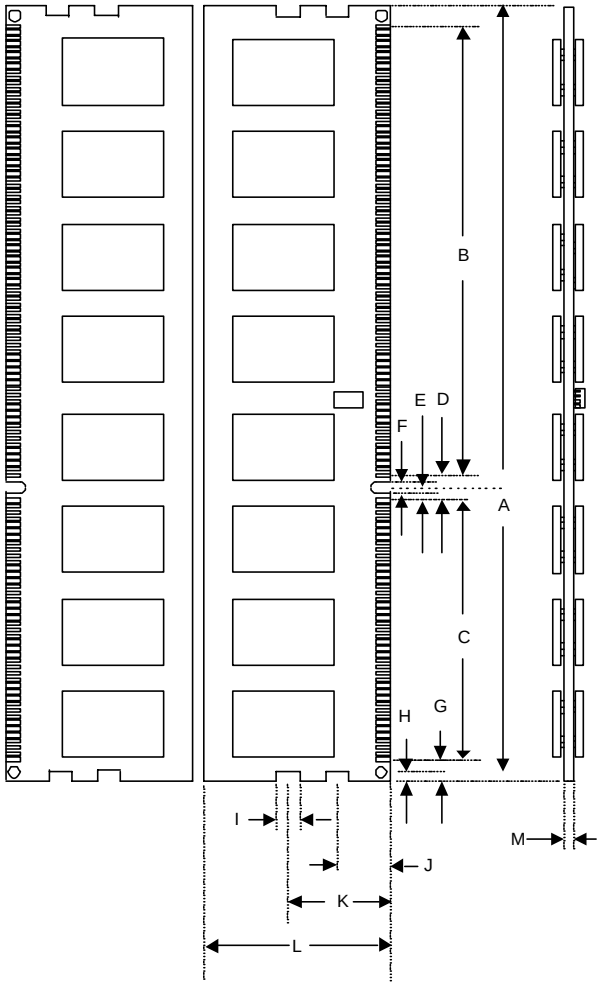
The TS256MLK64V1U is a 256M x 64bits DDR3-1066 Unbuffered DIMM. The TS256MLK64V1U consists of 16pcs 128Mx8 bits DDR3 SDRAMs in FBGA packages and a 2048 bits serial EEPROM on a 240-pin printed circuit board. The TS256MLK64V1U is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products
- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ=1.5V ± 0.075V
- Max clock Freq: 533MHz f_{ck}; 1066Mb/S/Pin.
- 8 independent internal bank
- Programmable CAS Latency: 6, 7, 8, 9
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 6
- 8-bits pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Asynchronous Reset
- Serial presence detect with EEPROM

Placement



PCB: 09-2830

Dimensions

Side	Millimeters	Inches
A	133.35±0.15	5.250±0.006
B	71	2.795
C	47	1.850
D	5	0.197
E	2.5	0.098
F	1.5±0.10	0.059±0.039
G	5.175	0.204
H	2.311	0.091
I	3±0.1	0.118±0.00394
J	9.5	0.374
K	17.3	0.681
L	30±0.15	1.181±0.006
M	1.27±0.10	0.050±0.004

(Refer Placement)

Pin Identification

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	DIMM rank select lines.
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
V_{REF}DQ	I/O reference supply
V_{REF}CA	Command/address reference supply
V_{DD}SPD	SPD EEPROM power supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	41	VSS	81	DQ32	121	VSS	161	NC	201	DQ37
02	VSS	42	NC	82	DQ33	122	DQ4	162	NC	202	VSS
03	DQ0	43	NC	83	VSS	123	DQ5	163	VSS	203	DM4
04	DQ1	44	VSS	84	DQS4	124	VSS	164	NC	204	NC
05	VSS	45	NC	85	DQS4	125	DM0	165	NC	205	VSS
06	DQS0	46	NC	86	VSS	126	NC	166	VSS	206	DQ38
07	DQS0	47	VSS	87	DQ34	127	VSS	167	NC***	207	DQ39
08	VSS	48	NC	88	DQ35	128	DQ6	168	Reset	208	VSS
09	DQ2	49	NC	89	VSS	129	DQ7	169	CKE1*	209	DQ44
10	DQ3	50	CKE0	90	DQ40	130	VSS	170	VDD	210	DQ45
11	VSS	51	VDD	91	DQ41	131	DQ12	171	A15	211	VSS
12	DQ8	52	BA2	92	VSS	132	DQ13	172	A14	212	DM5
13	DQ9	53	NC	93	DQS5	133	VSS	173	VDD	213	NC
14	VSS	54	VDD	94	DQS5	134	DM1	174	A12/BC	214	VSS
15	DQS1	55	A11	95	VSS	135	NC	175	A9	215	DQ46
16	DQS1	56	A7	96	DQ42	136	VSS	176	VDD	216	DQ47
17	VSS	57	VDD	97	DQ43	137	DQ14	177	A8	217	VSS
18	DQ10	58	A5	98	VSS	138	DQ15	178	A6	218	DQ52
19	DQ11	59	A4	99	DQ48	139	VSS	179	VDD	219	DQ53
20	VSS	60	VDD	100	DQ49	140	DQ20	180	A3	220	VSS
21	DQ16	61	A2	101	VSS	141	DQ21	181	A1	221	DM6
22	DQ17	62	VDD	102	DQS6	142	VSS	182	VDD	222	NC
23	VSS	63	CK1**	103	DQS6	143	DM2	183	VDD	223	VSS
24	DQS2	64	CK1**	104	VSS	144	NC	184	CK0	224	DQ54
25	DQS2	65	VDD	105	DQ50	145	VSS	185	CK0	225	DQ55
26	VSS	66	VDD	106	DQ51	146	DQ22	186	VDD	226	VSS
27	DQ18	67	VREFCA	107	VSS	147	DQ23	187	NC	227	DQ60
28	DQ19	68	NC	108	DQ56	148	VSS	188	A0	228	DQ61
29	VSS	69	VDD	109	DQ57	149	DQ28	189	VDD	229	VSS
30	DQ24	70	A10/AP	110	VSS	150	DQ29	190	BA1	230	DM7
31	DQ25	71	BA0	111	DQS7	151	VSS	191	VDD	231	NC
32	VSS	72	VDD	112	DQS7	152	DM3	192	RAS	232	VSS
33	DQS3	73	WE	113	VSS	153	NC	193	S0	233	DQ62
34	DQS3	74	CAS	114	DQ58	154	VSS	194	VDD	234	DQ63
35	VSS	75	VDD	115	DQ59	155	DQ30	195	ODT0	235	VSS
36	DQ26	76	S1*	116	VSS	156	DQ31	196	A13	236	VDDSPD
37	DQ27	77	ODT1*	117	SA0	157	VSS	197	VDD	237	SA1
38	VSS	78	VDD	118	SCL	158	NC	198	NC	238	SDA
39	NC	79	NC	119	SA2	159	NC	199	VSS	239	VSS
40	NC	80	VSS	120	VTT	160	VSS	200	DQ36	240	VTT

*Used for dual-rank UDIMMs; NC on single-rank UDIMMs.
**Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated.
***TEST(pin 167) used by memory bus analysis tools (unused on memory DIMMs).